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SYSTEM EVALUATION ITEM 0001 OF MICROPROCESSOR-BASED POWER CONDI--ETC(U)
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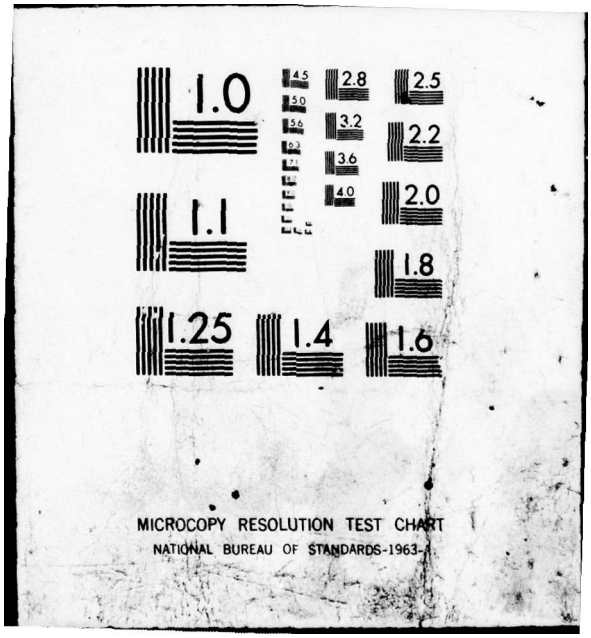
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LEVEL II

B.S.

SYSTEM EVALUATION

ITEM 0001

OF

MICROPROCESSOR-BASED POWER CONDITIONER CONTROLLER

CONTRACT NO. DAAK70-78-C-0117

PREPARED FOR

U. S. ARMY MERADCOM

FORT BELVOIR, VIRGINIA 22060

PREPARED BY

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SEPTEMBER 1978

37 p.

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1.0.0 SUMMARY

The results of an evaluation of a prototype 15 KW power conditioner, built by Delco Electronics, for MERADCOM are contained in this report. The evaluation was a prerequisite in the preparation for developing a microprocessor-based controller to replace an existing controller in the power conditioner.

The entire evaluation was performed by studying the Delco reports that are listed in Section 3 of this report. These are final and preliminary reports prepared by Delco for the U. S. Army. The power conditioner to be interfaced is currently being developed by Delco for MERADCOM at the Delco facility in Santa Barbara, California.

The primary objective of the evaluation was to obtain a thorough understanding of the power conditioner from studying the latest available documentation and to define the requirements for a microprocessor controller interface. This study will serve as the guideline for design of the baseline controller, the next task.

Although the new controller will interface to the existing sense signals satisfactorily, the capability of the microprocessor could enhance performance of the new controller if certain sense circuitry modifications were made. Suggestions and recommendations are included and discussed in this report.

2.0.0 PREFACE

The work described in this report was performed by Yucca International, Inc. under the direction of the U. S. Army Mobility Equipment Research and Development Command. This report completes the first task, of the first phase (CLIN 0001, Phase 1) of the U. S. Army contract no. DAAK-70-78-C-0117. The Contracting Officer's Representative is Dr. David Lee at the U. S. Army MERADCOM headquarters at Fort Belvoir, Virginia.

3.0.0 COPYRIGHT PERMISSION

The information contained in this report was derived from the following Government documents:

Source No. 1	Contract No. DAAK-02-72-C-0210 Frequency Converter Portable 10 KW	Final Report Vol. I	May 1974
Source No. 2	Contract No. DAAK-02-72-C-0210	Vol. II	May 1974
Source No. 3.	Contract No. DAAK-02-72-C-0210	Vol. III	January 1975
Source No. 4	Contract No. DAAK-70-77-C-0035 15 KW General Purpose Power Conditioner	Final Report AC-DC Section	April 1978
Source No. 5	Contract No. DAAK-70-77-C-0157 15 KW General Purpose Power Conditioner	Prelim. Report Inverter	July 1978
Source No. 6	MIL-STD-1332B		March 31, 1978

4.0.0 INTRODUCTION

The U. S. Army Mobile Equipment Research & Development Command (MERADCOM) has contracted with Yucca International, Inc. to perform Part 1 of Phase 1 to design, construct, and test a microprocessor-based controller for a general purpose 3 phase 15 KW power conditioner.

The new controller, when completed, will be capable of replacing the existing controller in a selected power conditioner to reduce cost, size, add new features, improve reliability and retain total system performance ability. An additional advantage is that it could easily be adaptable to other similar power conditioners.

The power conditioner selected by the Government is the one developed for the Army by Delco Electronics under contracts DAAK-02-72-C-0210 and DAAK-70-77-C-0035, and is continuing under contract DAAK-70-77-C-0157 at the Delco facility in Santa Barbara, California. When available, this power conditioner will be used for initial testing of the controller at Yucca. Final acceptance testing will be conducted at MERADCOM.

This is a report of the initial evaluation of the Delco 15 KW power conditioner. The information available consisted of several reports written by Delco for the Army. These are listed in Section 3. The results of this review outline a list of requirements for the baseline design using a microprocessor controller. Also included is a plan for the next task.

5.0.0 INVESTIGATION

5.1.0 REVIEW OF POWER CONDITIONER

5.1.1 OVERALL VIEW

The Delco 15 KW power conditioner can be described as a frequency changer. Frequency changers are useful for converting input power of one frequency to output power at another frequency. Frequency changers have been designed to derive power from an input source of varying frequency and amplitude (the output of the turbo alternator or diesel generator set for example) and provide at its output, AC power that is stable in frequency and has low distortion and good regulation.

Presently, the Delco 15 KW power conditioner is capable of deriving its power from 120/208 VRMS @ 50 Hz, 60 Hz, or 400 Hz three phase, which must be of utility class 2C (defined in MIL-STD-1332B) or better. The power conditioner is capable of providing quality AC output power at 120/240 VRMS @ 60 Hz or 400 Hz single phase, or 120/208 VRMS @ 60 Hz or 400 Hz three phase 3 or 4 wire. Table 1 lists the electrical requirements of the power conditioner and the measured performance.

Frequency conversion in the power conditioner is accomplished in three steps. The AC input is rectified to DC, the DC is converted to a higher DC voltage, and then the DC is inverted to produce an AC output. A brief description of each of these steps follows.

Each phase of the power input is rectified separately through bridge rectifiers. There is very little filtering performed on the DC at the output of the three bridge rectifiers. Since a resistive load is desired to minimize the introduction of harmonics back into the power source, filtering is kept to the minimum necessary for proper operation of the DC to DC converter that follows. The three DC to DC converters are identical and have been designed to appear as a resistive load and a switch to the bridge rectifiers that feed them.

The unregulated, unfiltered DC applied to a DC to DC converter is converted to high frequency sinusoidal voltage pulses and applied to the primary of a step-up isolation transformer. The pulses at the secondary are rectified and filtered to produce a positive and negative voltage with reference to an isolated common. The three DC to DC converter outputs are paralleled.

From the filtered, regulated, and isolated DC, and inverter constructs 3 phases of stair-step approximated sine waves and delivers them to triplen harmonic cancellation and filter circuitry.

5.1.2 AC TO DC TO DC SECTION

Figure 2 is a schematic of the AC to DC converter section. Shown are the 3 phase AC inputs, the 3 bridge rectifiers, and the 3 DC to DC converters described briefly in Section 5.1.1.

The DC to DC converters are referred to as 4 SCR resonant converters. Contained in a resonant converter are 4 SCR's connected to form a bridge type circuit. The output of the SCR bridge is connected to a series resonant load formed by a capacitor (C13 and C14), a choke (L9) and the primary of a step-up isolation transformer (T1).

The gates of the SCR's are fired in a fixed sequence by the power conditioner's controller at a frequency that is determined by load conditions. An increase in load requires an increase in frequency.

Q3 and Q2 are fired simultaneously to cause a half-sinusoid current pulse through the isolation transformer primary. Voltage at the secondary is rectified and filtered. The collapsing magnetic field causes CR3 and CR2 to conduct. This commutates off Q3 and Q2 for approximately 18 μs (well above the SCR spec requirements of 10 μs). A current transformer senses the current through CR2 and makes this signal available to the controller as a commutation sense signal. The sense signal indicates that the two SCR's are assumed to be turned off. To prevent causing a short circuit across the bridge rectifiers, the controller waits for the commutation sense signal before it permits the other pair of SCR's (Q1 and Q4) to be triggered

on. The magnetic field in the transformer must be allowed to collapse and the reverse energy produced must be removed before the application of another pulse. In other words, the frequency of operation must be kept below the resonant frequency of the converter. (The resonant frequency was not specified in the Delco reports.)

The frequency of operation necessary to produce 18 KW @ 300 VDC (± 150 VDC) into the inverter is 5119 Hz. (Actual three phase AC power out of the inverter with 18 KW in, is approximately 15 KW.) Table 2 provides more information concerning operating frequency vs. converter power output.

5.1.3 INVERTER

The inverter, supplied with the regulated DC input from the converter and crystal referenced waveform generation signals from the controller, will produce quality 3 phase AC output.

The waveform generation signals from the controller consist of gate driver signals for each of the 28 SCR's in the inverter. The controller does not provide commutation off signals because it is performed automatically by the inverter design and the SCR firing sequence.

Figure 4A is a simplified schematic of the inverter. Figure 4B is a simplified diagram of three phases of stair-step approximated sine waves. It can be seen that the SCR firing sequence for generating the center pulses in

Figure 4B is PB-, PA+, PC-, PB+, PA-, and PC+. These SCR's may be found in Figure 4A in a section of the inverter referred to as the power center.

Simultaneous with the firing of a power center SCR, a stair-step waveform must be started on both of the other phases. Conveniently, the stair-step voltages of both phases are the same polarity. This polarity may be applied to the top of the auto transformer by firing either T+ or T-. The stair-steps may be generated by, first, firing the appropriate phase select SCR's and then firing the appropriate left and right SCR's in the sequence that produces the desired results.

It is apparent from Figure 4 that the "right" SCR's are not configured properly to deliver a positive stair-step to the load. The same is true for the left SCR's if a negative stair-step is to be produced.

If a large output filter capacitance supplied current back into the inverter at the times described above, then forward bias across the SCR's can be achieved. The large filter capacitance causes the output current to lead the output voltage. (See Figure 5.) Immediately after the output current crosses zero (reverses directions), the conditions are correct for turning on the SCR's indicated.

To clarify, Delco has purposely introduced a leading power factor in the inverter output with a large filter capacitance. The leading power factor

is necessary to fire the step-forming SCR's when they would normally be reverse biased. The leading power factor must be maintained under all load conditions to successfully fire, and thus commutate off, all of the step-forming SCR's. Otherwise, distortion of the outputs will result.

The large filter capacitance is responsible for a 2 KW loss at no load. To reduce this loss, it appears Delco is considering using relays to reduce capacitance at minimum or no load.

Not shown in Figure 4A are 4 SCR's. For detailed information about the 4 SCR's or the inverter operation described, consult Source No. 5, p. 13-24.

5.1.4 VOLTAGE REGULATION

To maintain 120/208 VAC at the inverter output the converter must supply the inverter with approximately $\pm$ 140 VDC at a current that is determined by the load. It is important to note that the inverter does not provide the controller with any means of system voltage regulation or current limiting.

The controller must exercise these functions through control of the 12 SCR gate signals to the resonant converters.

The response time of the regulation loop will limit the ability to react to transients. An optimum amount of capacitance must be provided at the converter output to meet specified transient response requirements. Too much capacitance may cause damage to the inverter if an overload (or short circuit) occurs causing this uncontrolled current to flow through the low impedance inverter. Obviously, then, in the interest of protecting the inverter and meeting transient response requirements, the regulation loop must be fast.

5.2.0 REQUIREMENT FOR CONTROLLER BASELINE DESIGN

The requirements are:

1) Minimum use of analog components;
2) Optimize software control functions versus hardware control functions;
3) Failsafe operation;
4) Detection, protection, and error indication of power conditioner faults;
5) Provide the necessary timing signals to the converter SCR's to achieve sub-cycle voltage regulation and current limiting of the inverter output;
6) Short circuit current protection;
7) Provide for momentary overloads (up to 200% of rated load for 5 seconds) but then reduce to rated output to prevent internal damage.

8) Provide crystal referenced center pulse and step-forming timing signals to the 28 SCR's in the inverter. These timing signals will permit either 60 Hz or 400 Hz sine wave output;

9) Permit the power conditioner to supply 120/208 VRMS three phase @ 60 or 400 Hz or 120/240 VRMS single phase @ 60 or 400 Hz;

10) Reliable operation in electromagnetic environment of power conditioner;

11) Permit the output voltage to be adjusted -5%, +15% away from nominal;

12) Determine mode of operation by reading front panel switch settings;

13) Include all necessary power supplies;

14) Must not cause a degradation in performance;

15) Adaptable to other similar power conditioners;

16) Verify proper operation of power conditioner by monitoring the following available sense signals.

CONVERTER INPUT VOLTAGE SENSE - 3 Total

Each of the 3 AC input phases are sensed by a transformer and then rectified. These signals are monitored to detect input over-voltage, under-voltage, and lost phase. They are not involved directly with the controller regulation loop.

CONVERTER SCR COMMUTATION SENSE - 3 Total

A positive or negative voltage at the output of the sense circuit will indicate which pair of SCR's were just commutated off. There is one sense circuit per converter.

CONVERTER OUTPUT CURRENT SENSE - 3 Total

Each of the converter step-up isolation transformers secondary are sensed by a current transformer. This sense signal is rectified to provide a voltage approximately proportional to the direct current provided to inverter input.

CONVERTER OUTPUT VOLTAGE SENSE - 1 Total

The voltage between the + line and the - line is sensed through a voltage divider. No transformer is used.

INVERTER INPUT CURRENT SENSE - 1 Total

The + line and the - line each have inserted in them, a separate primary winding of the same current transformer. The output of the transformer is rectified.

INVERTER OUTPUT VOLTAGE SENSE - 3 Total

The sense signals provided are isolated from the output by a transformer and rectified.

INVERTER OUTPUT CURRENT SENSE - 3 Total

Each of the three output phases are sensed by a current transformer. Rectification is performed before the sense signal is made available to the controller.

The location of all sense signals discussed in this section are shown in Figure 1.

5.3.0 DESIRED CONTROLLER FUNCTIONS

The desired functions are:

1) Provide for a multi-character 7 segment display on the front panel. The display might be used to indicate mode of operation, self-test or diagnostic error conditions, fault conditions, etc.;
2) Sense over temperature;
3) Sense out-of-frequency;
4) Provide for controlled short circuit (time/overload profile);
5) Provide for 50 Hz output frequency option. (For NATO compatibility);
6) Consider self-test capability; for instance, check RAM, A/D's, D/A's, I/O (if applicable) etc. Determine if PROM'S are authorized by reading a code or checksum. Perform the self-test before power conditioner goes from standby to operate.

5.4.0 PLANS FOR NEXT TASK

Objective: Develop the controller baseline design. Determine and document the expected requirements and duties of the microprocessor(s), in preparation for microprocessor(s) selection.

1) Generate one or more conceptual approaches;
2) All conceptual approaches must conform to the requirements listed in 5.2.0;
3) The conceptual approaches will clearly define the controller to a functional block level. The necessary amount of RAM, ROM, and I/O will be approximated;
4) An analysis will be included that will highlight the advantages of the approach;
5) From the conceptual approaches, the best or a compromise will be selected for developing the baseline controller;
6) The baseline design will be documented with
   a) Detailed schematic (portions may be functional blocks);
   b) List of microprocessor(s) duties;
   c) Narrative description of the more difficult software routines that will be needed.

A good feel should be obtained for what the microprocessor is expected to perform. This is necessary for the selection of the optimum processor(s), the third task.

6.0.0 DISCUSSION

This discussion will focus on the problems and difficulties encountered during this task.

An analysis of the firing sequence of the 6 pairs of SCR's was determined by studying the schematic on page 6-11, Source No. 4. The 6 lines leaving the schematic on the right are believed to be mislabeled. Each of these signals carry a 12 μs pulse to circuitry that will fire a pair of SCR's in one of the three resonant converters in Figure 4. The firing sequence is believed to be Phase A Q3, Q2; Phase C Q1, Q4; Phase B Q3, Q2; Phase A Q1, Q4; Phase C Q3, Q2; Phase B Q1, Q4. The period between the pulses are dependent on the operating frequency or a commutation sense failure.

A definition of the operating frequency is believed to be the reciprocal of the period between pulses to the same pair of converter SCR's. At an operating frequency of 5119 Hz, for example, the period would be 195 μs (unless a commutation failure occurred causing all pulses to be delayed 10 ms).

The operating frequency can be misleading when thinking in terms of the resonant frequency. When the period of the operating frequency is 195 μs, the actual time between pulses to the resonant load is 195 ÷ 2 or 97.5 μs, for an effective frequency of twice the operating frequency. The actual

time between pulses to the resonant load must never decrease below 18 μs which is approximately the time needed to turn off a converter SCR.

Part 1 of Phase 1 of the contract will concentrate on developing the hardware and software necessary to perform voltage regulation of the power conditioner. The converter operating frequency (control frequency) may be based on either the inverter output voltages or the converter output voltage or both.

The inverter output voltage can be regulated more accurately by sensing the inverter outputs instead of the converter output, but response time of the regulation loop is sacrificed, since it takes longer to sense 3 outputs instead of one.

Unless a DC average of the inverter output voltages are measured, the value will have to be correlated to some point on the sine wave for comparison to a sine table stored in memory (In addition to verifying correct output voltage, sampling in this manner will check distortion.) Performing the above measurements on the output and determining a control signal, could take a significant amount of time.

The nomimal inverter output voltage is 120 VRMS line to neutral, which corresponds to approximately $\pm$ 140 VDC at the converter output. This relationship may change slightly at different output frequencies or loads.

Regulating the converter output to produce an accurate approximation of the inverter output voltage could prove challenging if load or frequency dependent variables exist in the inverter. The problem can partially be corrected by storing in computer memory a "load profile." Perhaps a load profile will be stored for each output frequency. The load profile will permit the controller to make slight adjustments to the converter output voltage to correct for changes in the inverter under various loads. Implementing this load profile will necessitate sensing the inverter input current.

The existing inverter output voltage and current sense signals are routed through isolation transformers and then rectified to produce two positive half sine waves. The forward diode drops may introduce an error when the inverter output is crossing zero. This may produce an error at all inverter voltages. Being able to identify the positive and negative half-cycle of the inverter output voltage is useful and this identification is more difficult when these signals are rectified. To achieve the accuracy desired, it may be necessary to sense these voltages and currents more directly.

The inverter output voltages measured must be correlated somehow to their exact position on the sine wave. There are several methods of achieving this (and these will be investigated during the next task).

7.0.0 CONCLUSIONS

In general, from the data review, a thorough understanding of the power conditioner has been obtained. The requirements and plans for the next task, the controller baseline design, have been formulated and included in this report.

An objective for the controller baseline design is to improve performance. The capability of the microprocessor-based controller to improve performance over that of the existing controller may be enhanced by changes to existing inverter output voltage and current sense circuitry. Appropriate recommendations will be made after the next task.

A requirement of the controller is to provide sub-cycle regulation response. Due to the complexity and time required to measure the inverter output voltages, it may be desired to base the converter control frequency initially on converter output voltage and then optimize with results of the inverter output measurements.

8.0.0 RECOMMENDATIONS

1) Based on the study during this period, it is recommended that we proceed immediately to the baseline design;
2) The baseline design should show any recommended changes in sensing circuitry;
3) A technical conference be held at Yucca International at the conclusion of the baseline design period for the purpose of review and concurrence with the baseline design.

9.0.0 DISTRIBUTION

Three copies to -- W. David Lee, DRDME-EA

Two copies to -- John A. Gabby, DRDME-PE-1

INPUT CHARACTERISTIC PARAMETER			MIL-STD-1332 PRECISE (CLASS 1)	MIL-STD-1332 UTILITY (CLASS 2)	PURCHASE DESCRIPTION	MEASURED PERFORMANCE	COMMENTS/ OTHER
1) Frequency Changer Input Voltage			N/A	N/A	120/208V +10%, -15%	120/208V +10%, -15%	Complies
2) Frequency Changer Input Frequency			N/A	N/A	50, 60, 400 Hz	60 Hz was tested	Not limited by design
3) Frequency Changer Input Current (60 Hz input frequency)	THD		N/A	N/A	5% over normal load range	3.5% at RL only	Limited (See Note A)
	Worse Single Harmonic		N/A	N/A	2% over normal load range	3.5%, 5th harmonic, RL only	Limited (See Note A)
	Deviation Factor		N/A	N/A	5% over normal load range	Not tested	See Note A
	Peak inrush on application of rated load from no load		N/A	N/A	Not specified	125% of rated load input current 125 ms rec. time	Adequate, but PD does not specify
4) Frequency Changer Input Power Factor (60 Hz input frequency)			N/A	N/A	Not specified	Unity (<3° leading)	Adequate, but PD does not specify
5) Converter Output Format (same as Inverter Input)			N/A	N/A	±150 Vdc, 60A (nom. at RL)	±150 Vdc, 60A (nom. at RL)	Complies
6) Voltage Regulation		60 Hz 400 Hz	1% 1%	3% N/A	1.5% 1.5%	<0.5% <0.5%	Complies
7) Steady State Stability	Short term (30 sec)	60 Hz 400 Hz	1% 1%	2% N/A	1% 1%	<0.5% <0.5%	Complies
	Long term (4 hrs)	60 Hz 400 Hz	2% 2%	4% N/A	1% 1%	<0.5% < 0.5%	Complies
8) Transient Performance	Application of rated load, dip	60 Hz 400 Hz	15%/0.5 sec 12%/0.5 sec	20%/3 sec N/A	20%/2 sec 20%/2 sec	13.7%/250 ms 12.3%/250 ms	Complies
	Rejection of rated load, rise	60 Hz 400 Hz	15%/0.5 sec 12%/0.5 sec	20%/3 sec N/A	20%/2 sec 20%/2 sec	17.5%/250 ms 17.9%/250 ms	Complies
	Dip for low power factor load	60 Hz 400 Hz	30%/0.7 sec 25%/0.7 sec	40%/5 sec N/A	40%/5 sec 40%/5 sec	2.5%/100 ms 60A/-0.07 PF Not measured	Complies

TABLE 1: PART 1 OF 2

9) Waveform	Total Harmonic Distortion	60 Hz 400 Hz	5% 5%	5% N/A	5% 5%	2.0% 2.05%	Complies
	Max Individual Harmonic	60 Hz 400 Hz	2% 2%	2% N/A	2% 2%	1.6%/5th 1.3%/5th	Complies
	Deviation Factor	60 Hz 400 Hz	5% 5%	5% N/A	5% 5%	<5% <5%	Complies
	Voltage Modulation (or ripple)	60 Hz 400 Hz	- -	- N/A	3V pk-pk (L-N) 3V pk-pk (L-N)	<0.5V <0.7V	Complies
10) Voltage Unbalance with Unbalanced Load		60 Hz 400 Hz	5% 5%	5% N/A	5% 5%	<1.5% <3.0%	Complies (see Note B)
11) Phase Balance Voltage		60 Hz 400 Hz	1% 1%	1% N/A	Not specified Not specified	<1% <1%	Complies with 1332 Precise
12) Voltage Adjustment Range		60 Hz 400 Hz	-5, +15% -5, +10%	-5, +15% N/A	±5% ±5%	Not tested Not tested	Not limited by design (should be -5, +15%)
13) Short Circuit Current		60 Hz 400 Hz	- -	- N/A	2 PU rated 2 PU rated	~1.5 PU ~1.5 PU	Device limited and control problem (see Note C)
14) All Output Frequency Parameters		60 Hz 400 Hz	- -	- N/A	60 Hz 400 Hz	60.01 Hz 400.08 Hz	Crystal reference complies
15) Phase Angle Balance		60 Hz 400 Hz	- -	- N/A	Not specified Not specified	<1 degree <1 degree	Adequate, but PD does not specify
16) Frequency Changer No/Load Losses		60 Hz 400 Hz	N/A N/A	N/A N/A	500 watts 500 watts	1828 watts 2676 watts	Does not comply
17) Frequency Changer Efficiency at Full Load (1.0 PF)		60 Hz 400 Hz	N/A N/A	N/A N/A	80% 80%	77% (Note D) 75% (Note D)	Does not comply
18) Frequency Changer Efficiency at Rated Load (0.8 PF)		60 Hz 400 Hz	N/A N/A	N/A N/A	80% 80%	80% (Note D) 77% (Note D)	Does not comply

NOTES:

A: THD with the frequency changer delivering rated load at 60 Hz or 400 Hz is 3.5%. If total harmonic content is referenced to the corresponding (i.e., rated) input current THD is somewhat greater at lower loads – approximately 7% at no load. The worst single harmonic increases likewise – to approximately 5% at no load.

B: Regulator instability, which can be corrected, was noted.

C: Rectifiers at the output of the ac-dc converter are underrated for output currents in excess of 150% of rated load output current. Regulator instability, which can be corrected, was noted.

D: This efficiency does not take into account loss contribution of power for cooling and low level power supplies for logic, contactors, lamps, etc. This would result in an approximately 2% overall reduction in efficiency.

TABLE 1: PART 2 OF 2

Comparison of Electrical Performance With Electrical Specifications

REPRODUCED FROM INVERTER PRELIMINARY DESIGN, CONTRACT NO. DAAK70-77-C-0157, P. 71

RESONANT CONVERTER OPERATING FREQUENCY (HZ)	CONVEPTEP POWEP OUTPUT (WATTS)
5119	18000
3459	12000
1726	6000
911	3000
345	1100

TABLE 2: RESONANT CONVERTER FREQUENCY VS. CONVEPTEP POWER OUTPUT

This information was obtained from Final Report AC-DC Section, Contract No. DAAk70-77-C-0035, P. 7-5

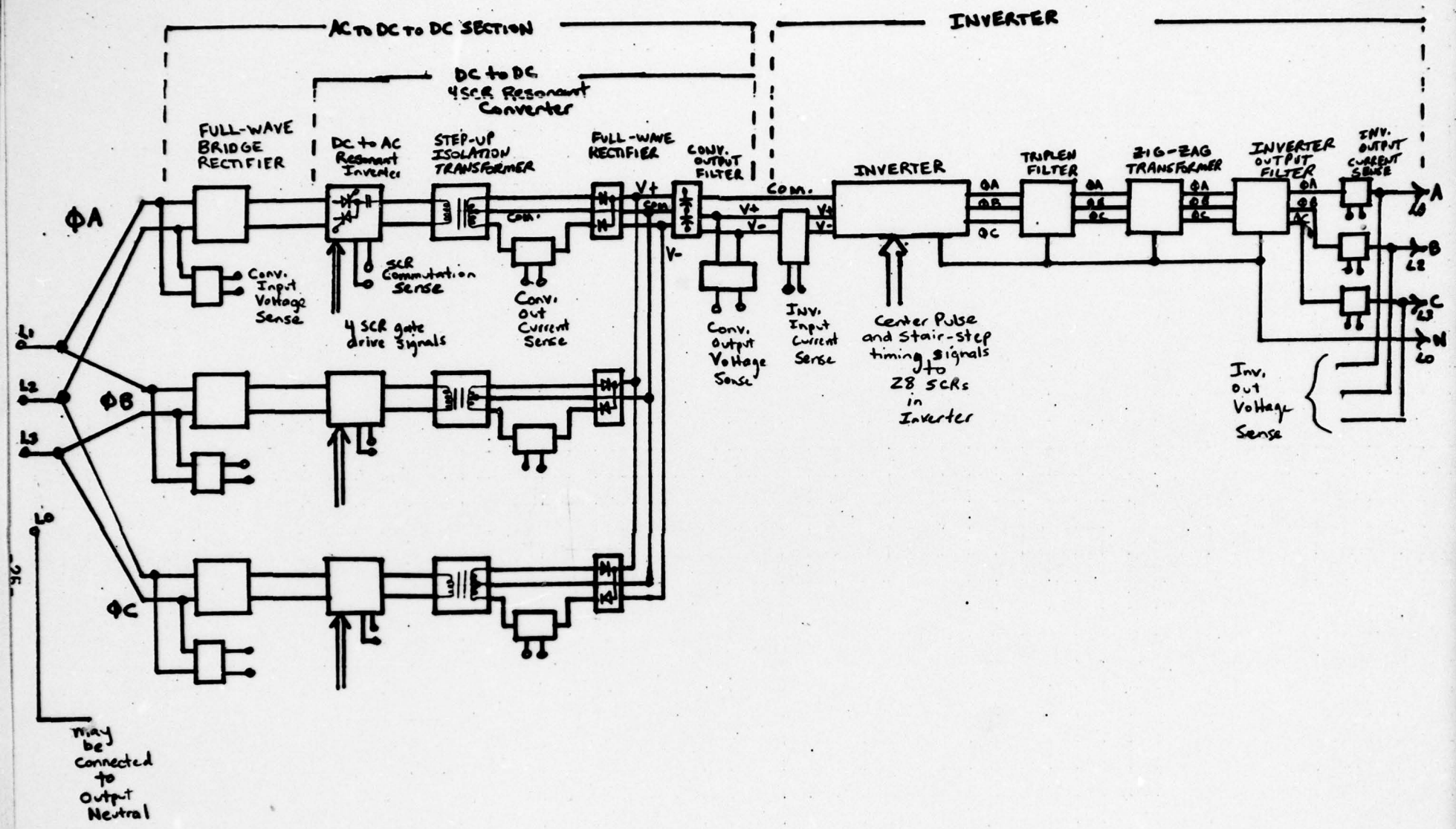


FIGURE 1: DELCO 15 KW POWER CONDITIONER (BLOCK DIAGRAM)

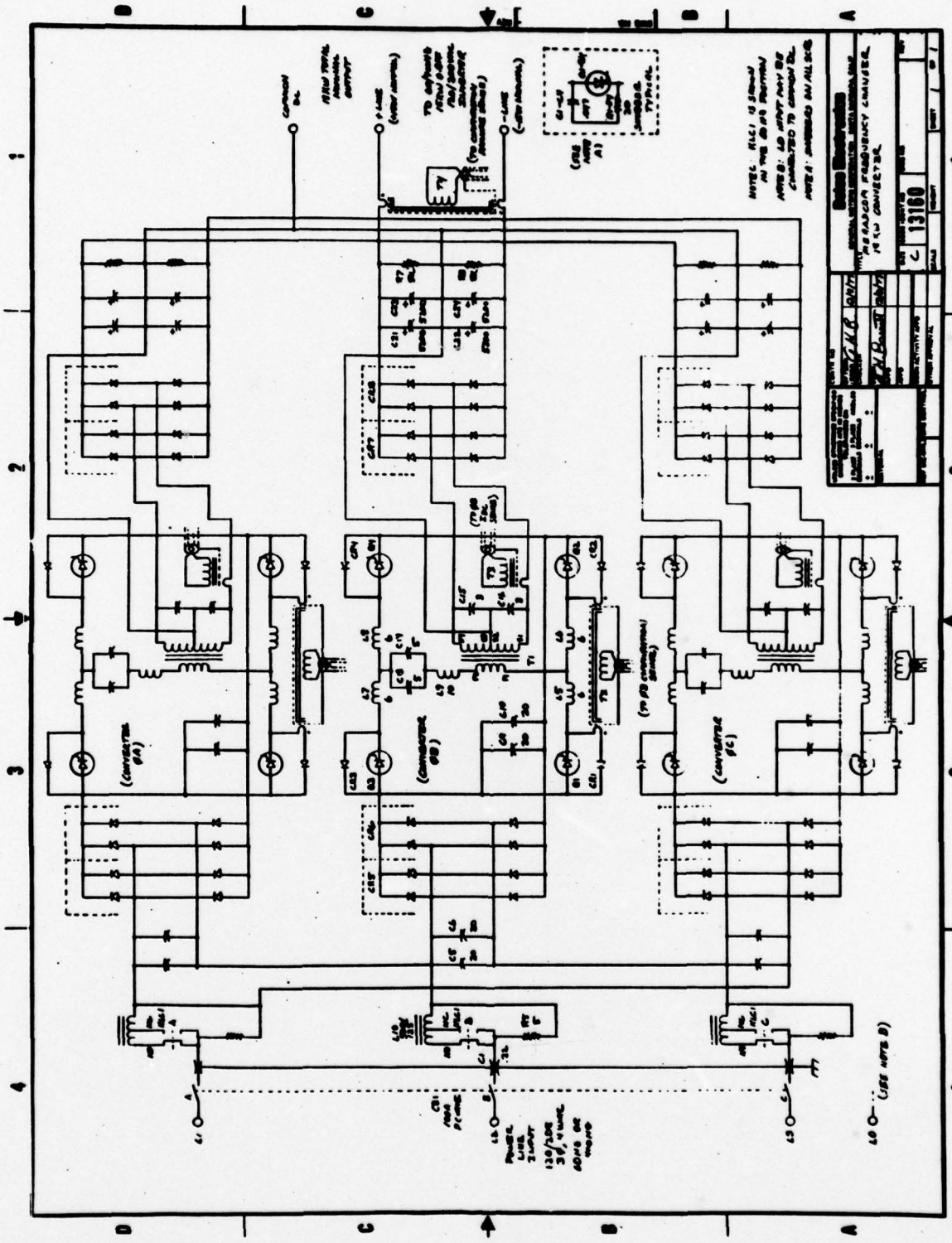


FIGURE 2: AC-DC CONVERTER FOR THE DELCO 15 KW POWER CONDITIONER

Reproduced from Inverter Preliminary Design, Contract No. DAAK70-77-C-0157, P. 69

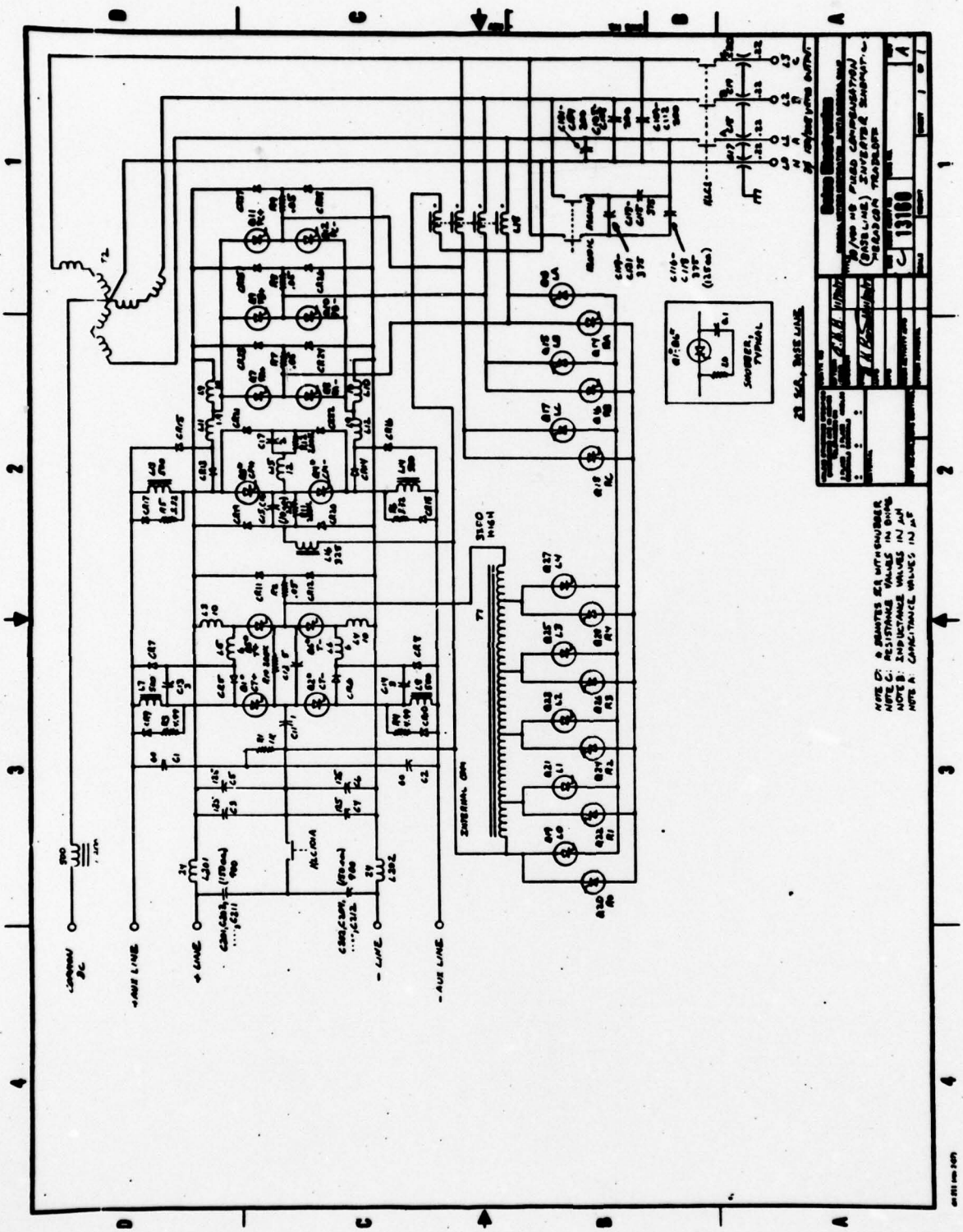


FIGURE 3: INVERTER FOR THE DELCO 15 KW POWER CONDITIONER

Reproduced from Inverter Preliminary Design, Contract No. DAAK70-77-C-0157, P. 70

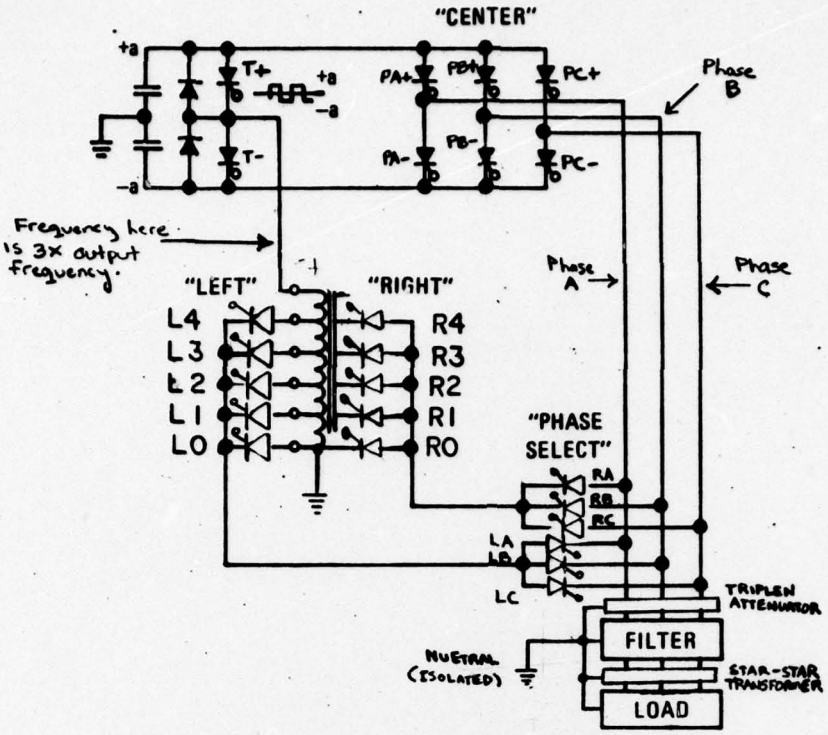


FIGURE 4A: SIMPLIFIED SCHEMATIC OF INVERTER

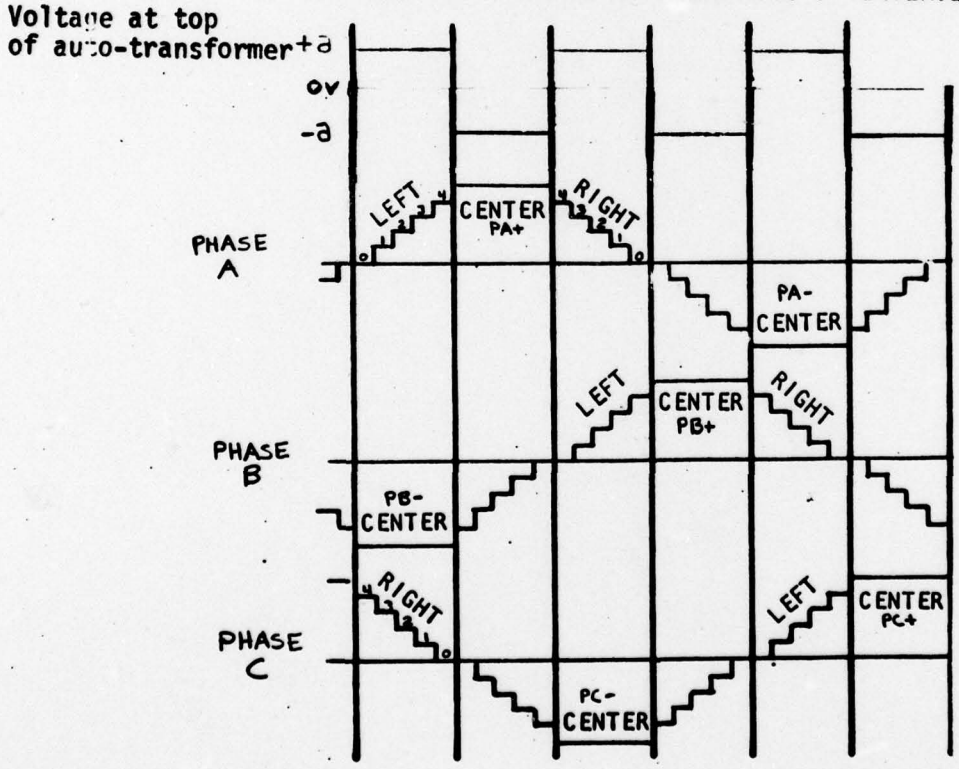


FIGURE 4B: SIMPLIFIED DIAGRAM OF STAIR-STEP SINE WAVES

Reprodueed and modified from Inverter Preliminary Design, Contract No. DAAK70-77-C-0157, P. 14

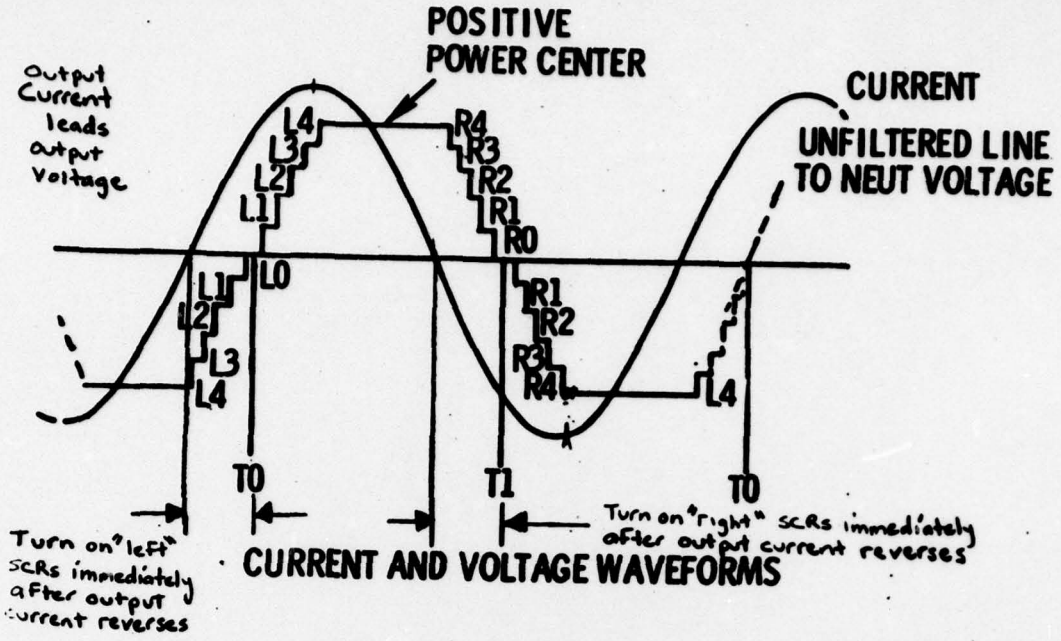


FIGURE 5: SIMPLIFIED INVERTER OUTPUT CURRENT AND VOLTAGE WAVEFORMS

Reproduced and modified from Inverter Preliminary Design, Contract No. DAAK70-77-C-0157, P. 23

APPENDIX A

8/18/78

FROM: Bill Tuten

SUBJECT: Trip Report- Meradcom visit on Contract DAAK-70-78-C-0117

Meeting with Dr. David Lee and Bob Williams

Bob Williams discussed the Delco Inverter System and how it operates. We then discussed how a microprocessor controller can be used in this inverter. The following information was gained:

Delco Inverter System

1) Present inverter has not been married to converter;
2) Efficiency of present inverter/converter combination is 75% not the spec 80% or the desired 85%;
3) Total system is large in size and heavy;
4) System appears to be very reliable;
5) Meradcom seems very pleased with the Delco System;
6) No fuses in system.

Desired Controller functions

1) Diagnostic;
2) Over/under voltage - both input and output
3) Out of frequency;
4) Over temperature;
5) Controlled short circuit (Time/overload profile)
6) Indicate status of input/output on display. If done display must have blocking option;

7) Look at preventive maintenance -- like pressure drop across air cleaner -- slowing down of fan, etc.

8) Monitor SCR status signals on when supposed to be -- not on otherwise.

Helpful documents

1) Look at ADA035043 (obtainable from Defense Documentation Center) Volumes 1, 3, and 5.

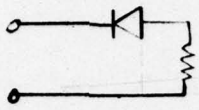
Unanswered questions

1) Response time?

2) Do all three converters regulate and operate at same frequency or all signals independent for each of the three converters?

Attached is a list of questions discussed.

QUESTION 1 What type of loads are expected to be powered with the inverter? In addition to motors and pure resistive loads, will we have loads similar to those shown below?



ANSWER 1 The inverter is very low impedance and, therefore, should be no problem with any type of load.

QUESTION 2 How is overload going to be handled? Limit to rated output or complete shut down.

ANSWER 2 Operates to 200% overload at 0^{o}pf and 95% bus voltage -- must shut down or back off after a time profile based upon overload.

QUESTION 3 What portion of the power converter can be shut down under microprocessor control without damage to other components or functional blocks.

ANSWER 3 Frequency shut down could be a problem. There should be no other problems. Also discuss that no fuses used in system. Only breaker is a magnetic breaker.

QUESTION 4 How long will the storage capability of the inverter handle momentary increases in load requirements? What is the response time required of the converter (regulator)?

ANSWER 4 At this time this answer is not known. It will be discussed with Delco.

QUESTION 5 In the event of minor failure that prevents the microprocessor from controlling the AC output to produce rated specification, will emergency back up measures be desired as an alternative to complete shut down? (For example: switching ROM in place of RAM to control inverter SCR's; or analog regulator as an alternate to digital loop in the event of failure)

QUESTION 6 How much diagnostic capability is desired? For example: self-test could indicate to front panel display, failing RAM memory address, a bad bit in one of the D/A's or A/D's, faulty DC to DC converter, etc.

ANSWERS 5, 6 Questions 5 and 6 concern failures, self-test and diagnostics. The answers to these questions have already been addressed in the body of this report.

APPENDIX B

Requests for additional information concerning the power conditioner were made to MERADCOM during a telephone conversation with Dr. David Lee on August 30, 1978, and will be included in the baseline design when received.

1) Updated charts and timing charts similar to those of Appendix A & B, respectively, in the purchase description;
2) Are transformers shown on page 6-15 of Source No. 4 the same transformers shown on page 6-13 of Source No. 4? If so, are the cards the transformers are on CCAA3 of CCA4?
3) To fire a converter SCR, it appears that both ends of a center-tapped primary are grounded sumultaneously for 12 μs. Is this correct?
4) Page 9-5 of Source No. 4 does not indicate any converter input voltage sense circuits. Where do the sense circuits shown on page 18 of Source No. 4 perform this function?
5) What is the resonant frequency of the DC to DC converters?